

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

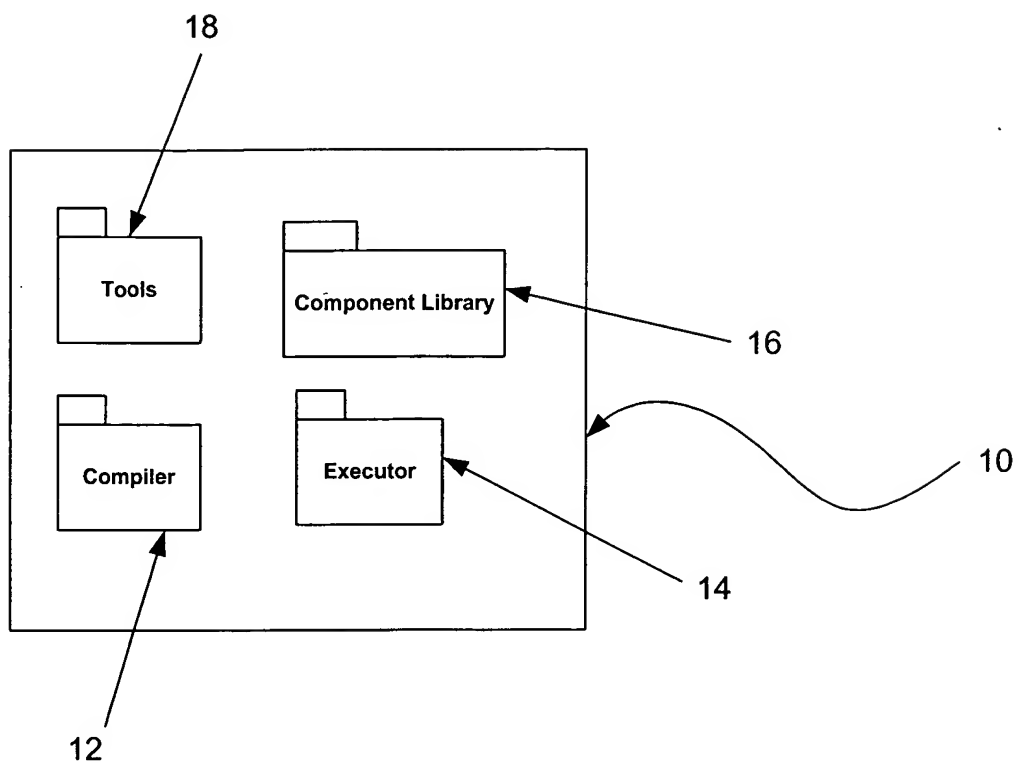
Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

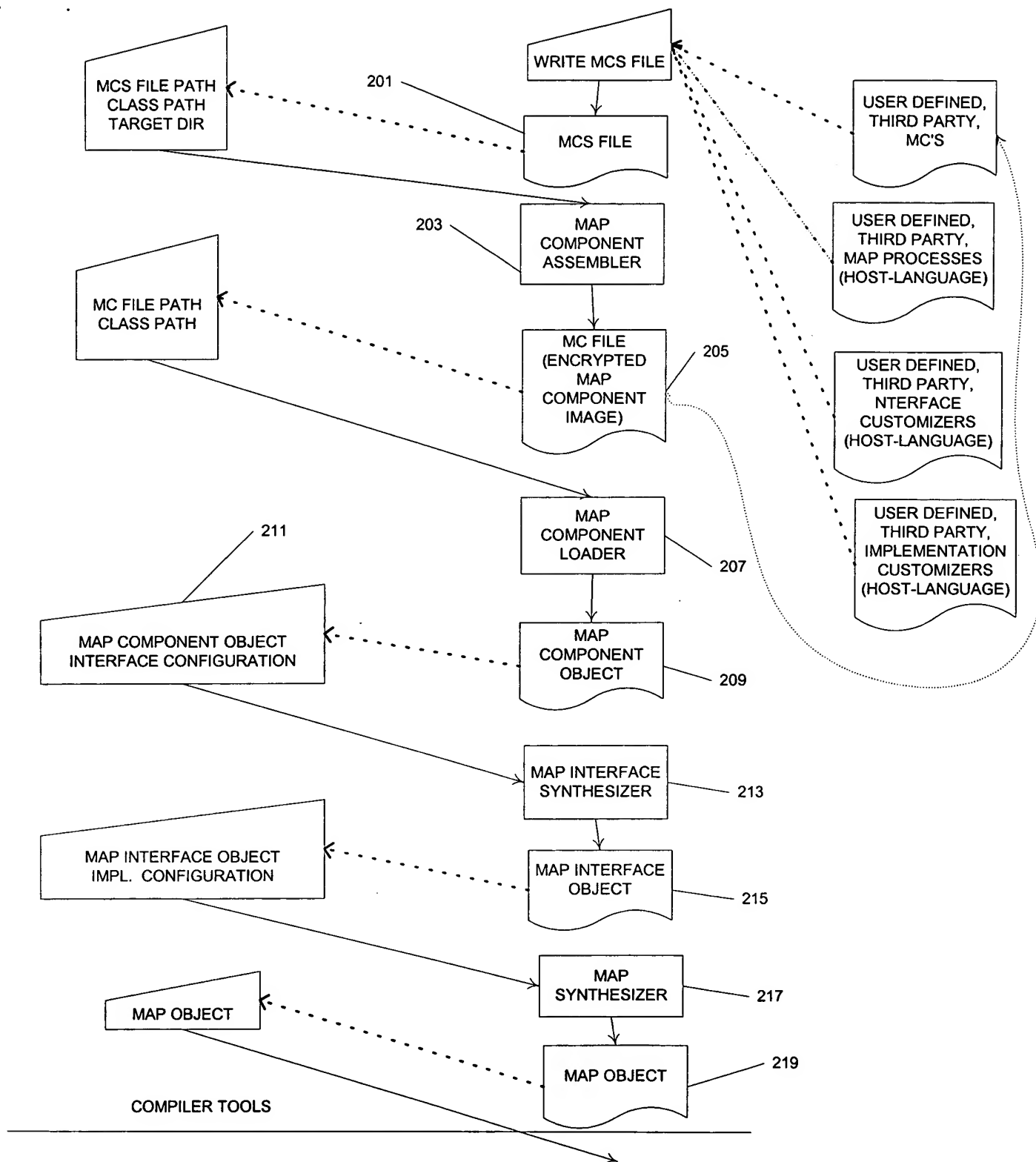
*IMAGE CUT OFF FIG. 11*

**IMAGES ARE BEST AVAILABLE COPY.**

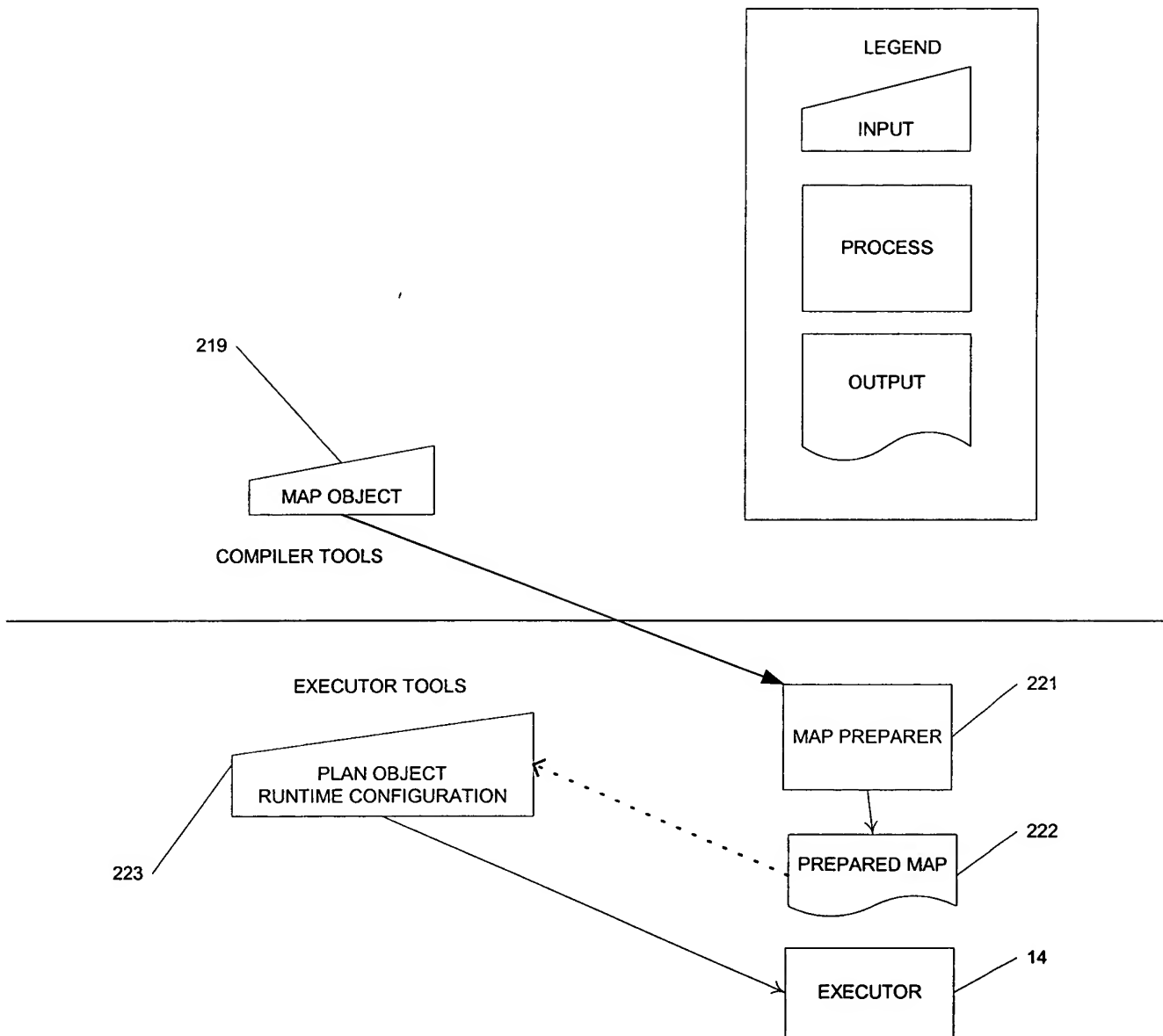
**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**



**Fig. 1**

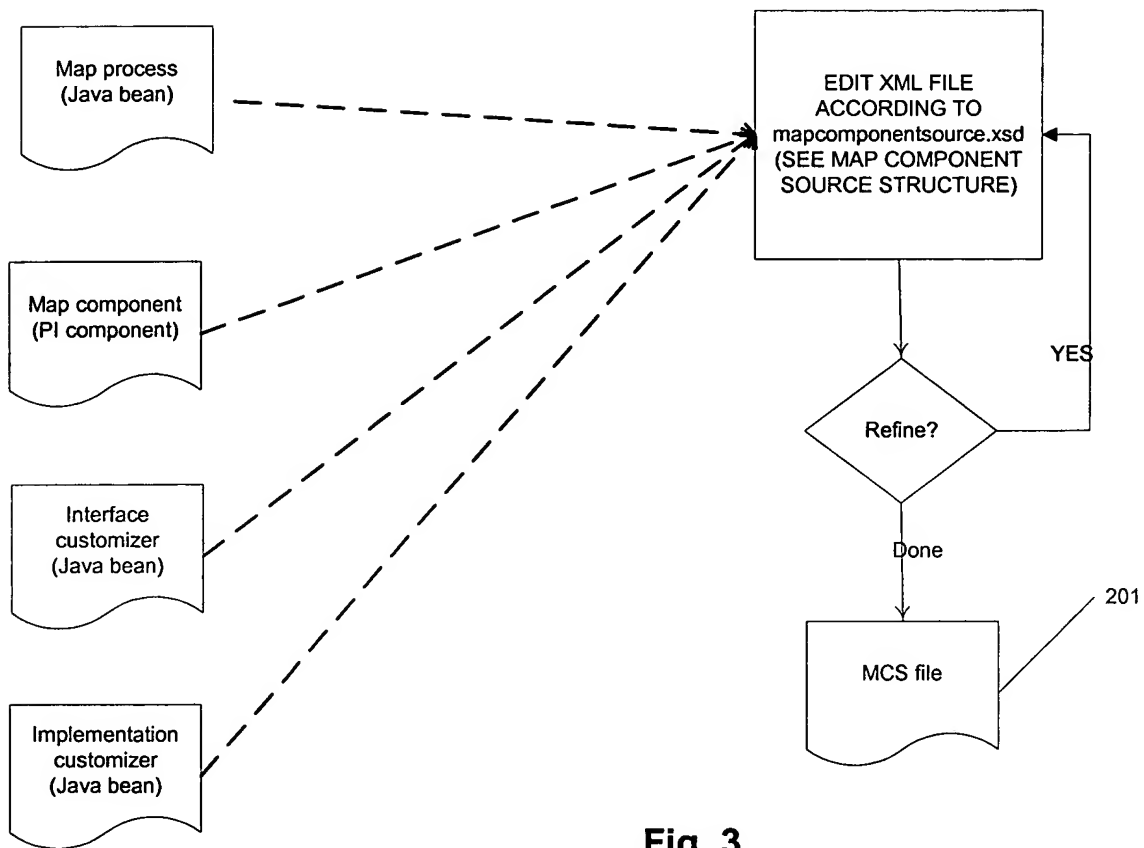


**Fig. 2A**



**Fig. 2B**

# MAP COMPONENT SOURCE CREATION



**Fig. 3**

Fig. 4

201

## ***INTERFACE***

DOCUMENTATION

INTERFACE PROPERTY LIST  
IMPLEMENTATION PROPERTY LIST  
RUNTIME PROPERTY LIST

PORT DECLARATION LIST ...

CUSTOMIZER DECLARATION AND  
CONFIGURATION

## ***IMPLEMENTATION***

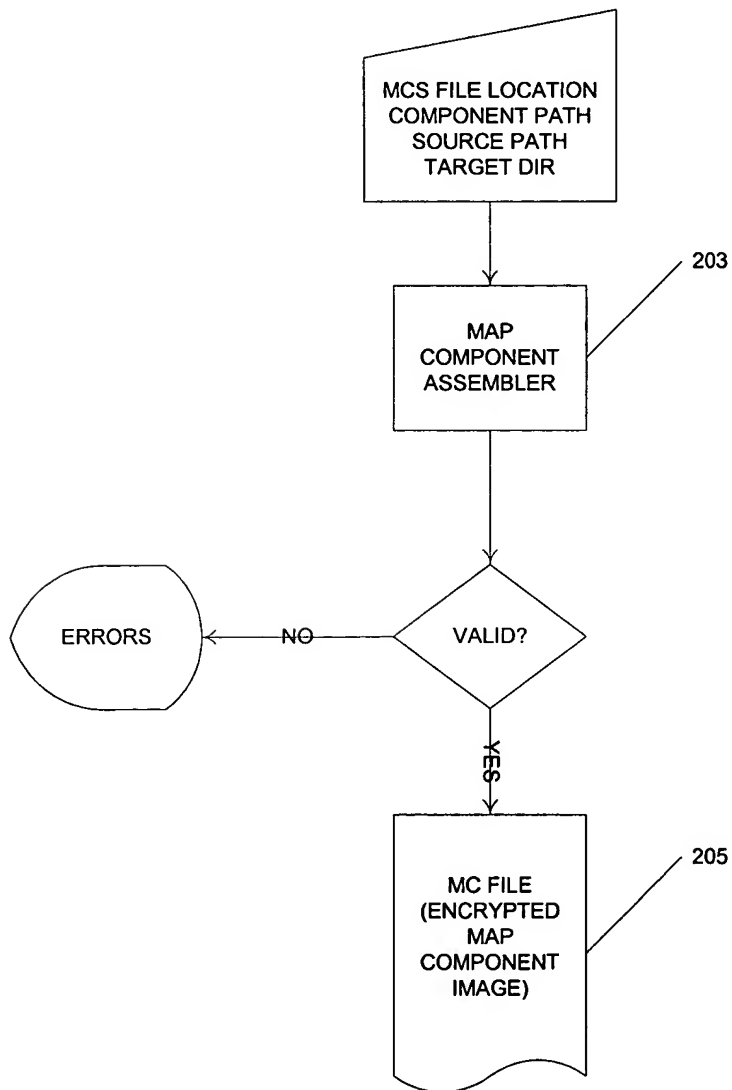
INTERNAL MAP COMPONENT INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

INTERNAL MAP PROCESS INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

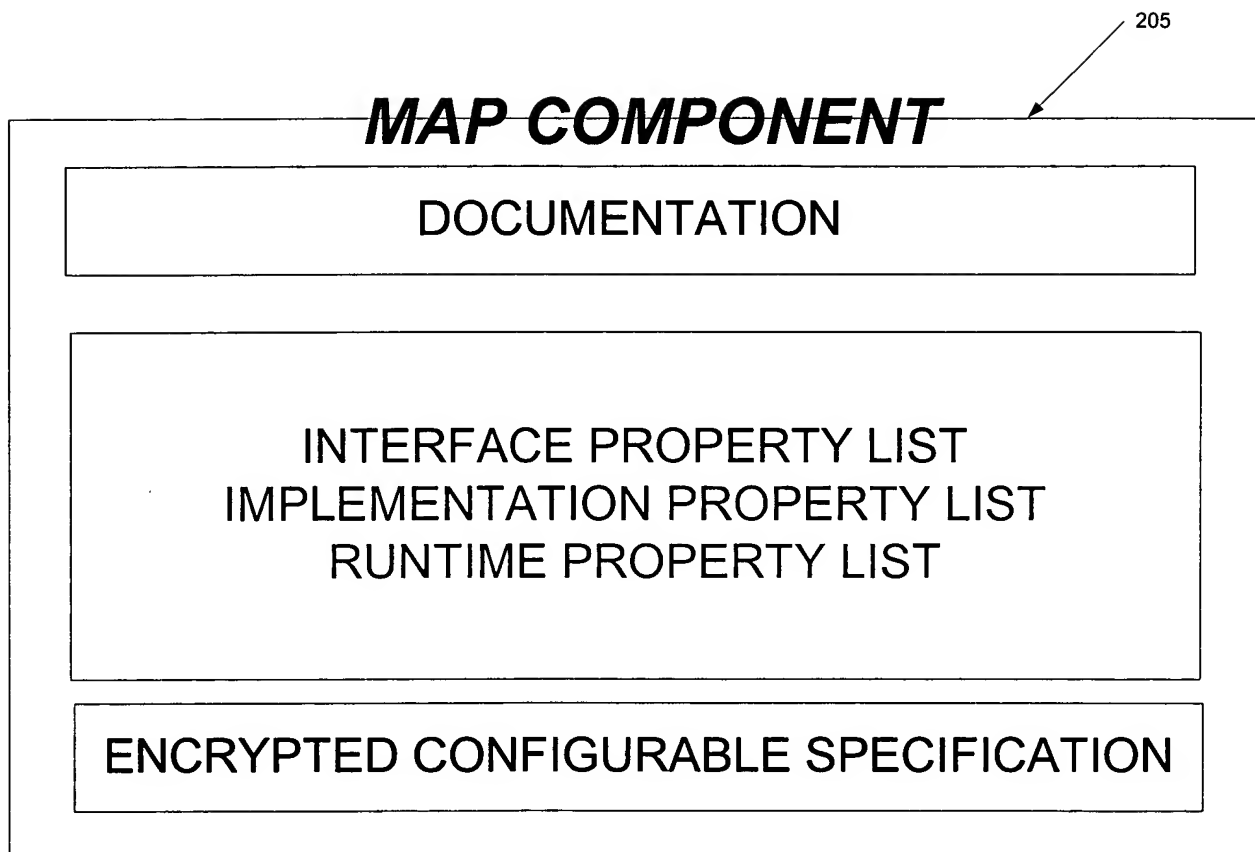
PORT TO PORT LINK LIST...

CUSTOMIZER DECLARATION AND  
CONFIGURATION

# MAP COMPONENT ASSEMBLY PROCESS



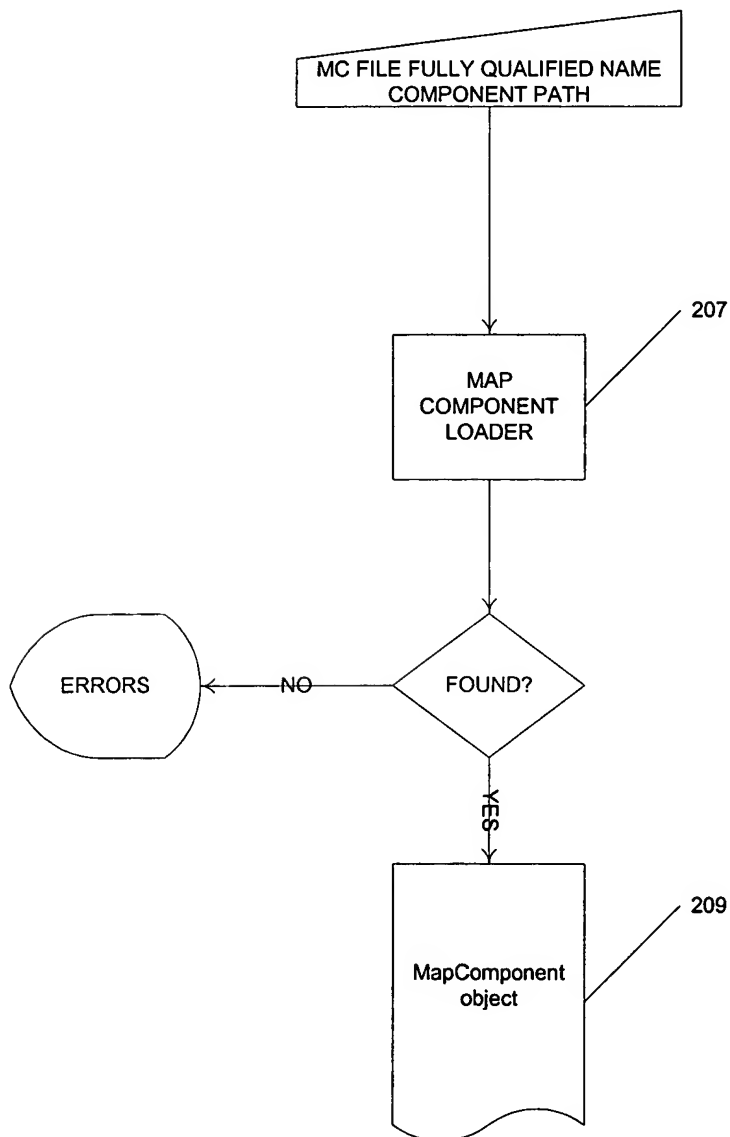
**Fig. 5**



**Fig. 6**

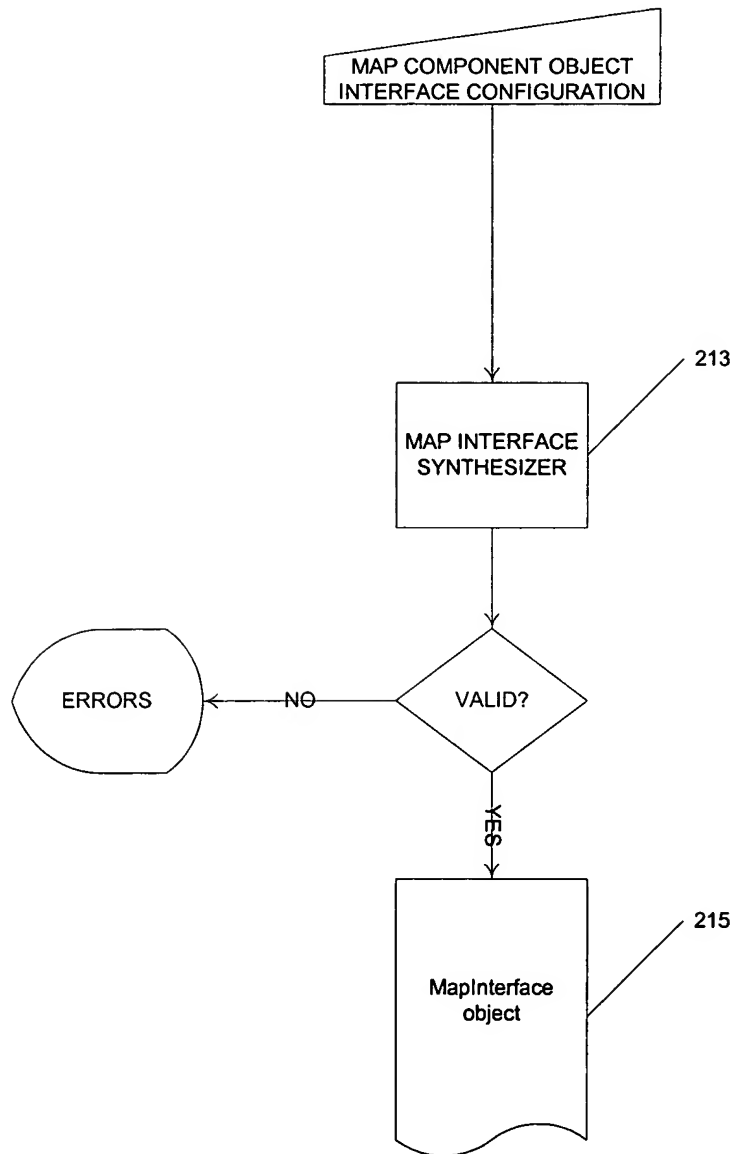


# MAP COMPONENT LOADING

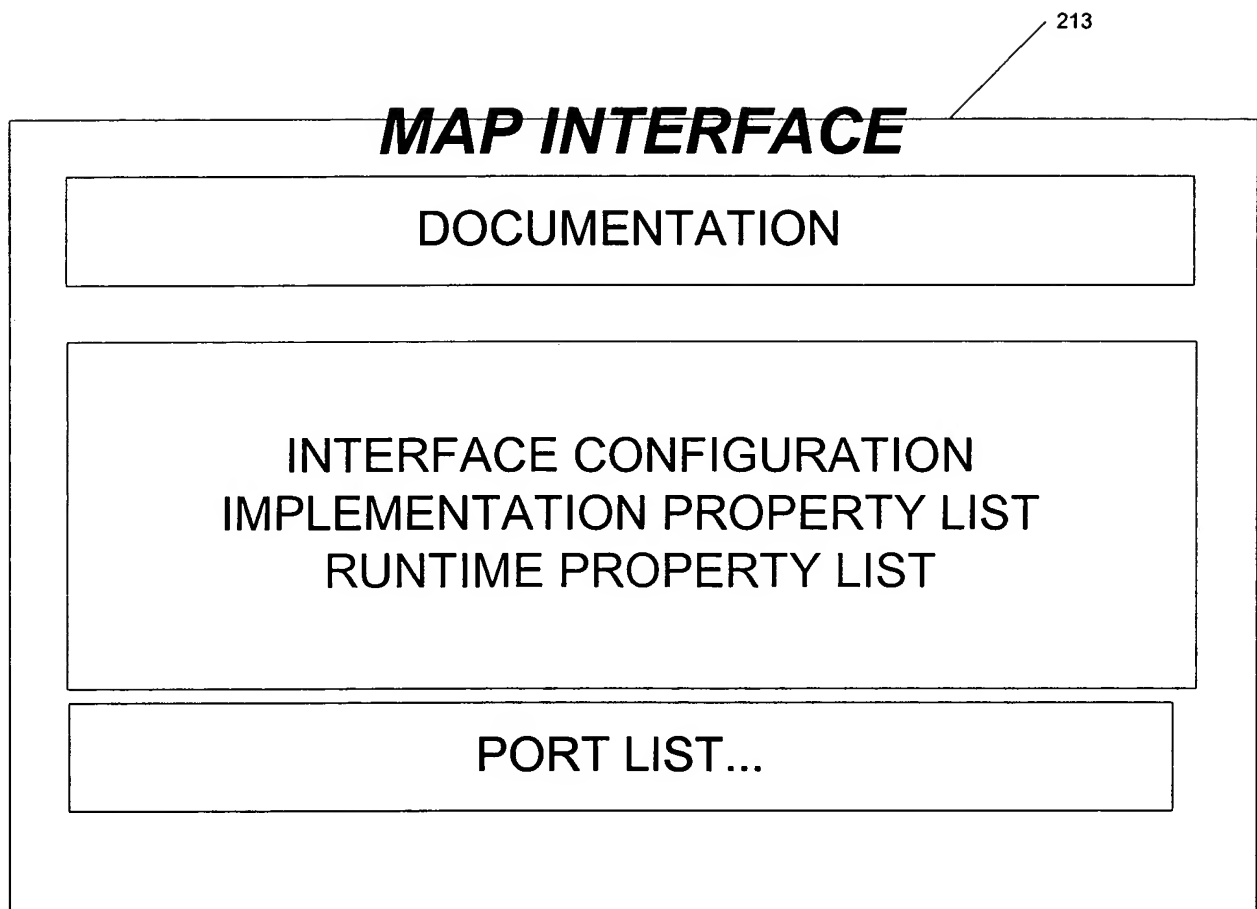


**Fig. 7**

# MAP INTERFACE SYNTHESIS

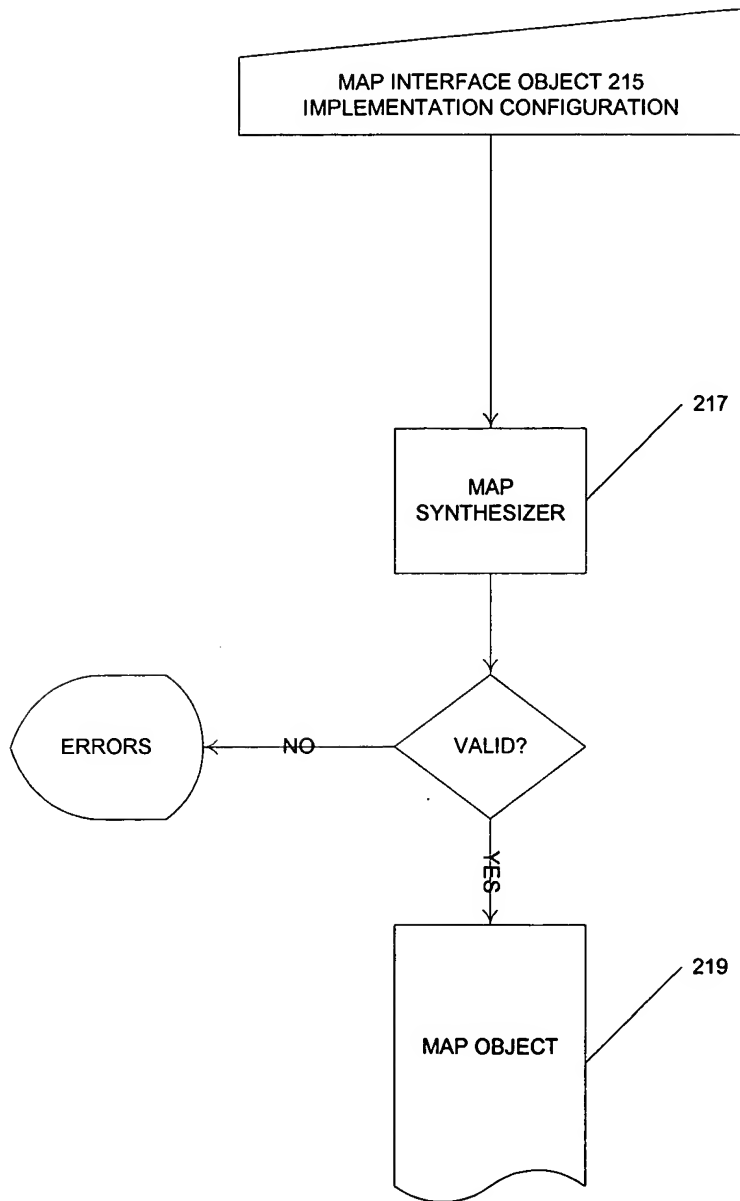


**Fig. 8**



**Fig. 9**

# MAP SYNTHESIS



**Fig. 10**

**MAP**

DOCUMENTATION

INTERFACE CONFIGURATION  
IMPLEMENTATION CONFIGURATION  
RUNTIME PROPERTY LIST

**INTERFACE**

PORT DECLARATION LIST ...

**IMPLEMENTATION (if open)**

INTERNAL MAP COMPONENT INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

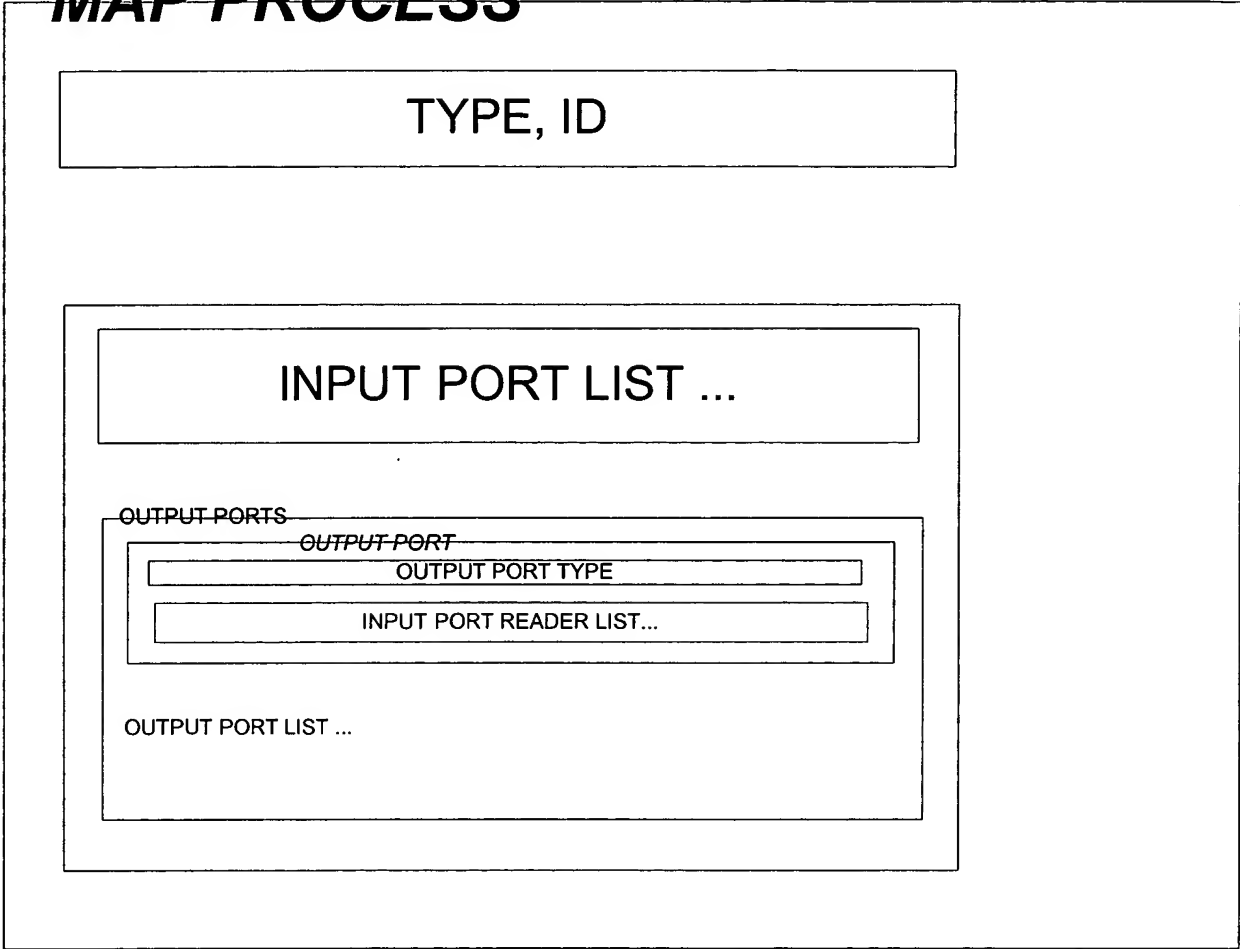
INTERNAL MAP PROCESS INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

PORT TO PORT LINK LIST...

INTERNAL MAP LIST...

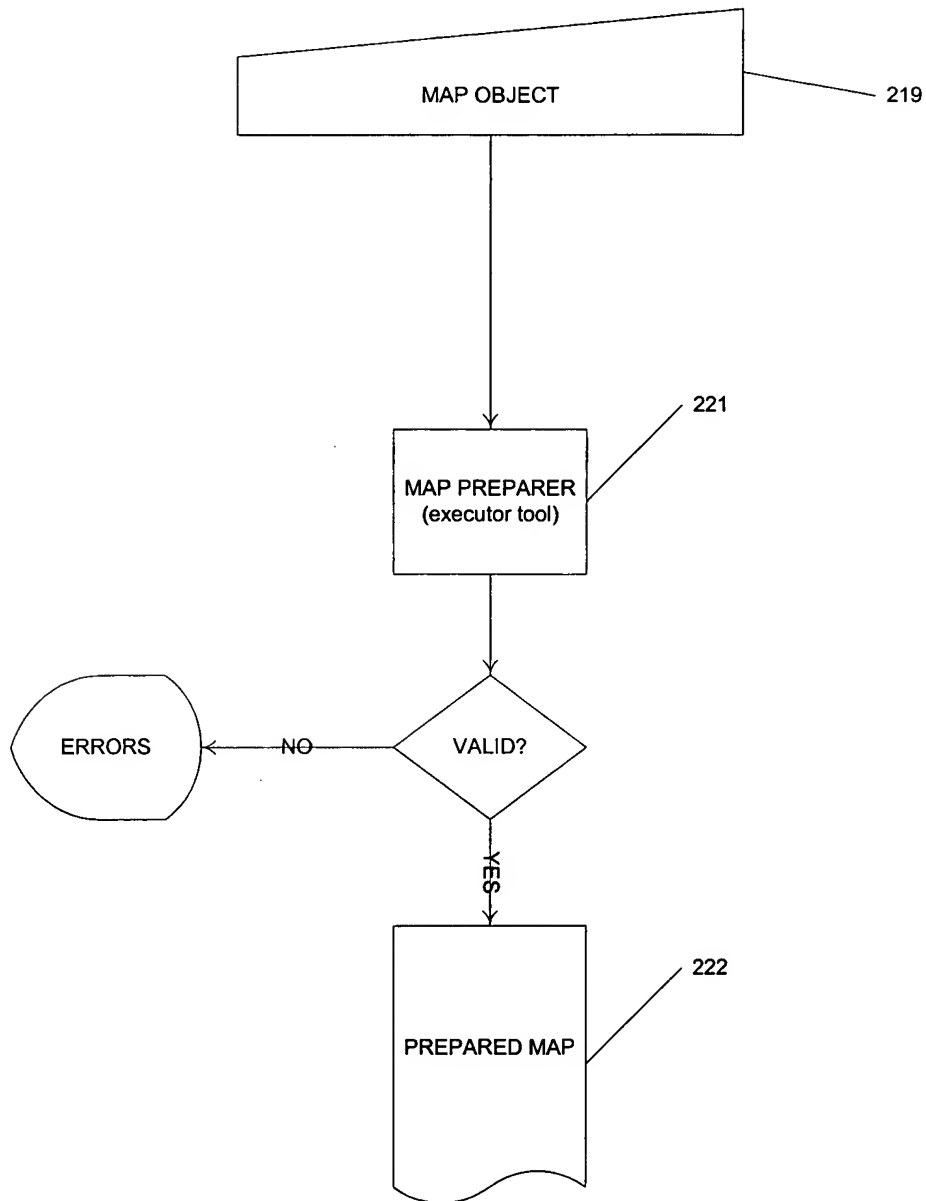
Fig. 12

**MAP PROCESS**



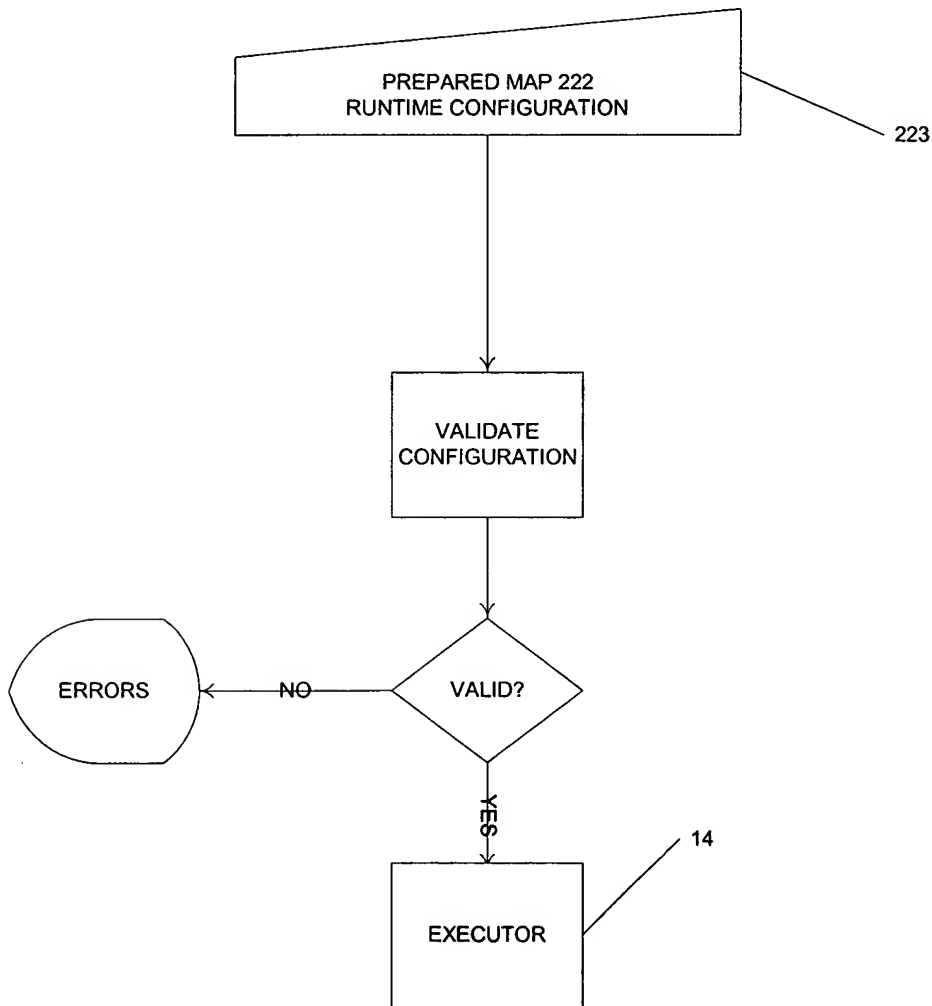
MAP PROCESS LIST ...

# MAP PREPARATION



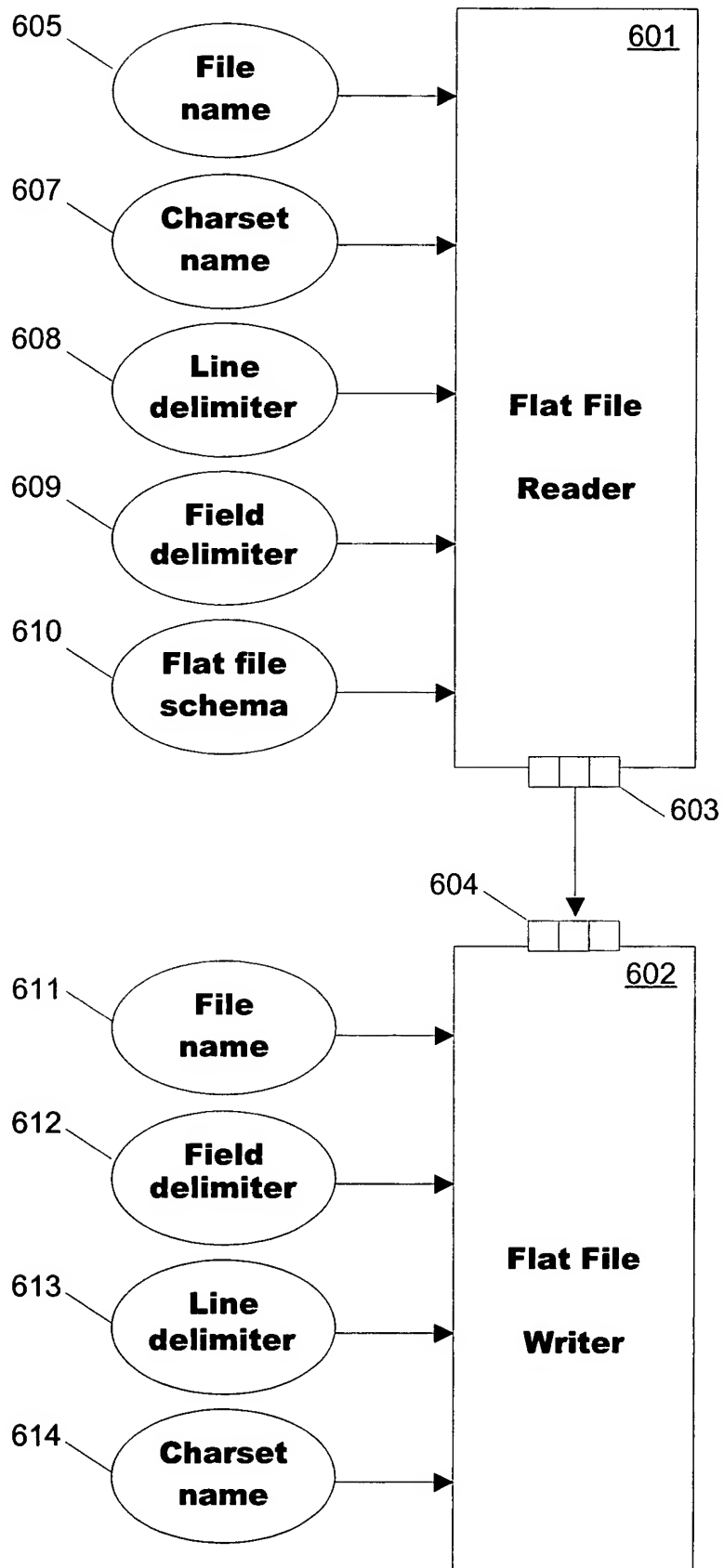
**Fig. 13**

# PREPARED MAP EXECUTION

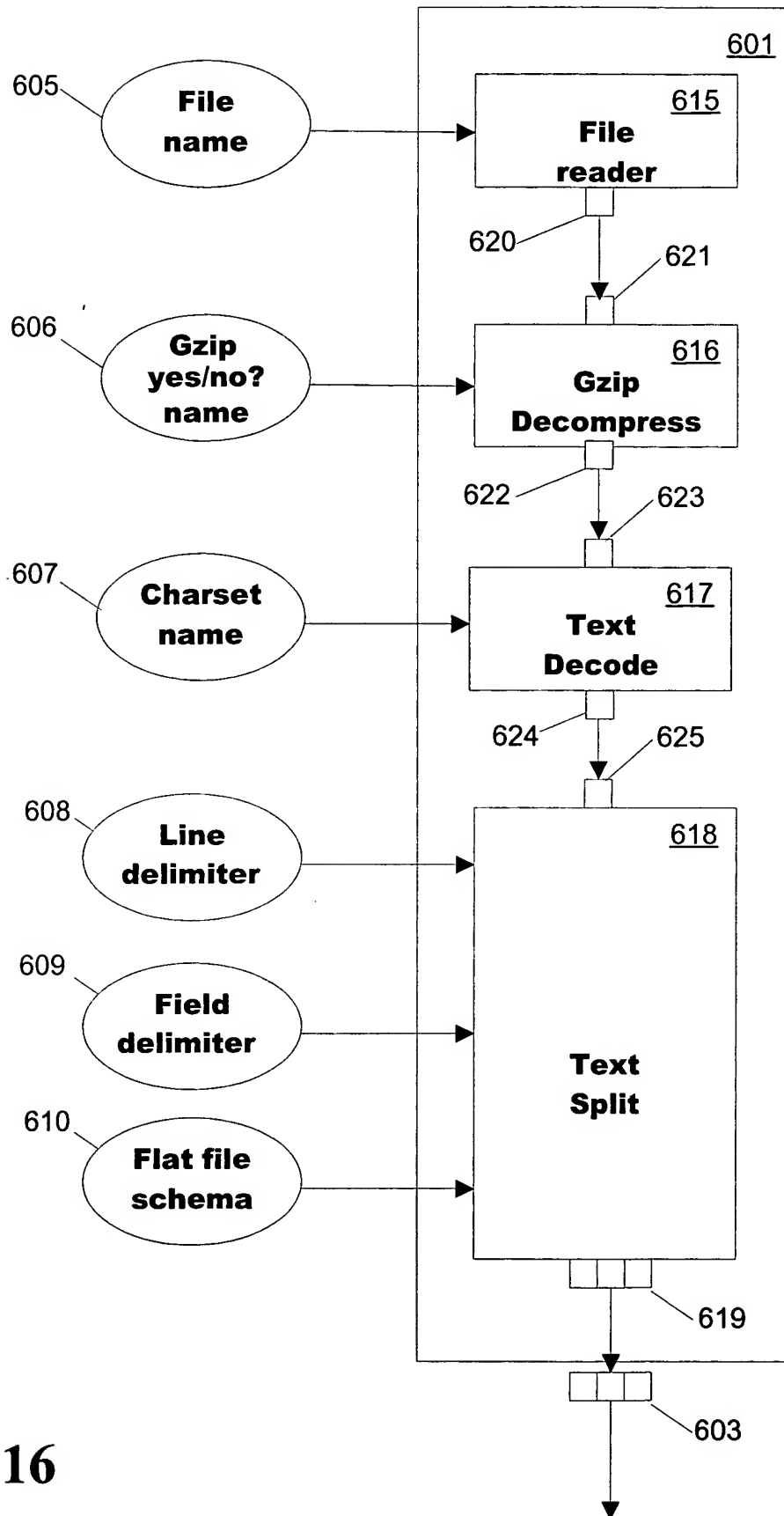


**Fig. 14**

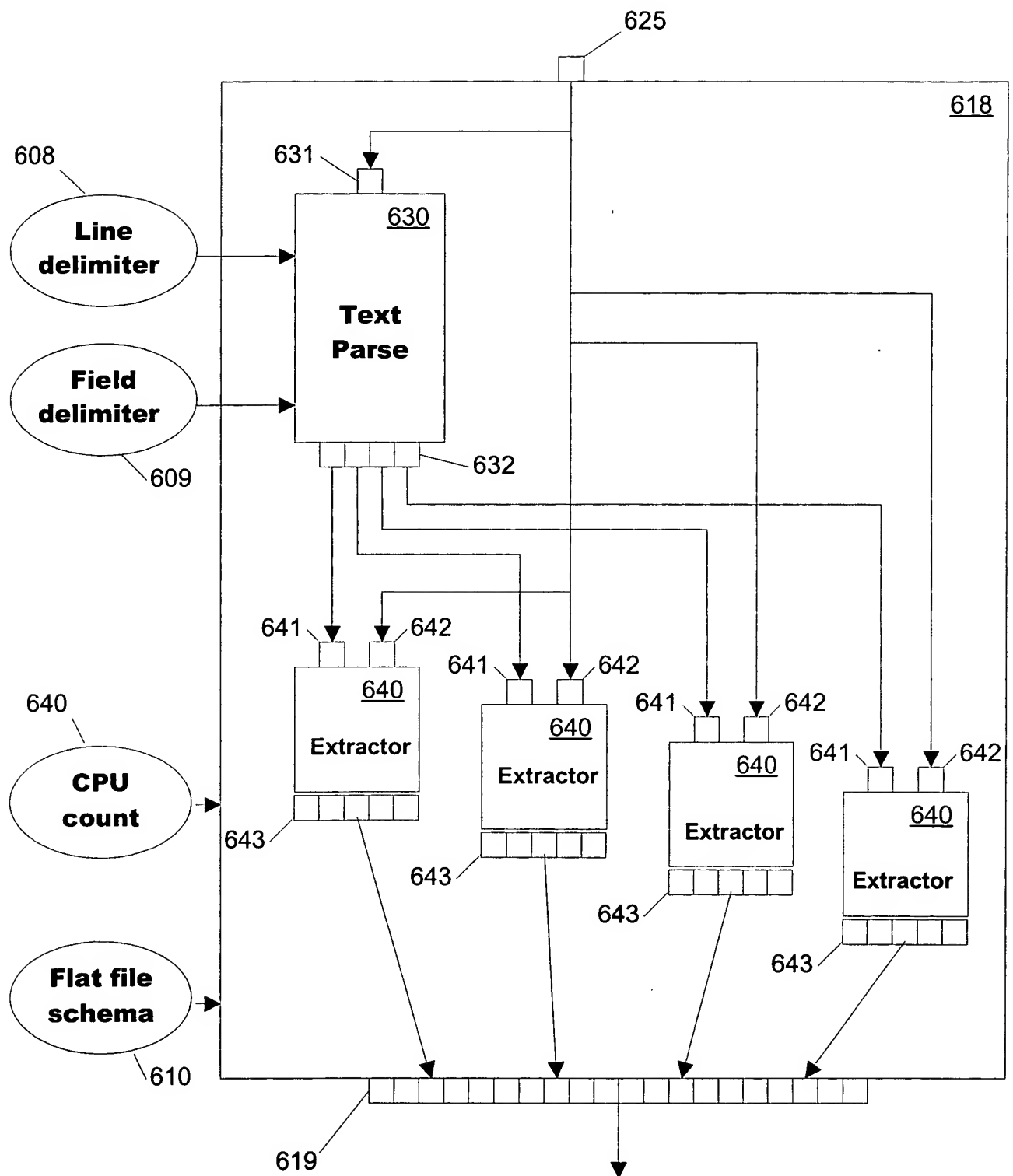




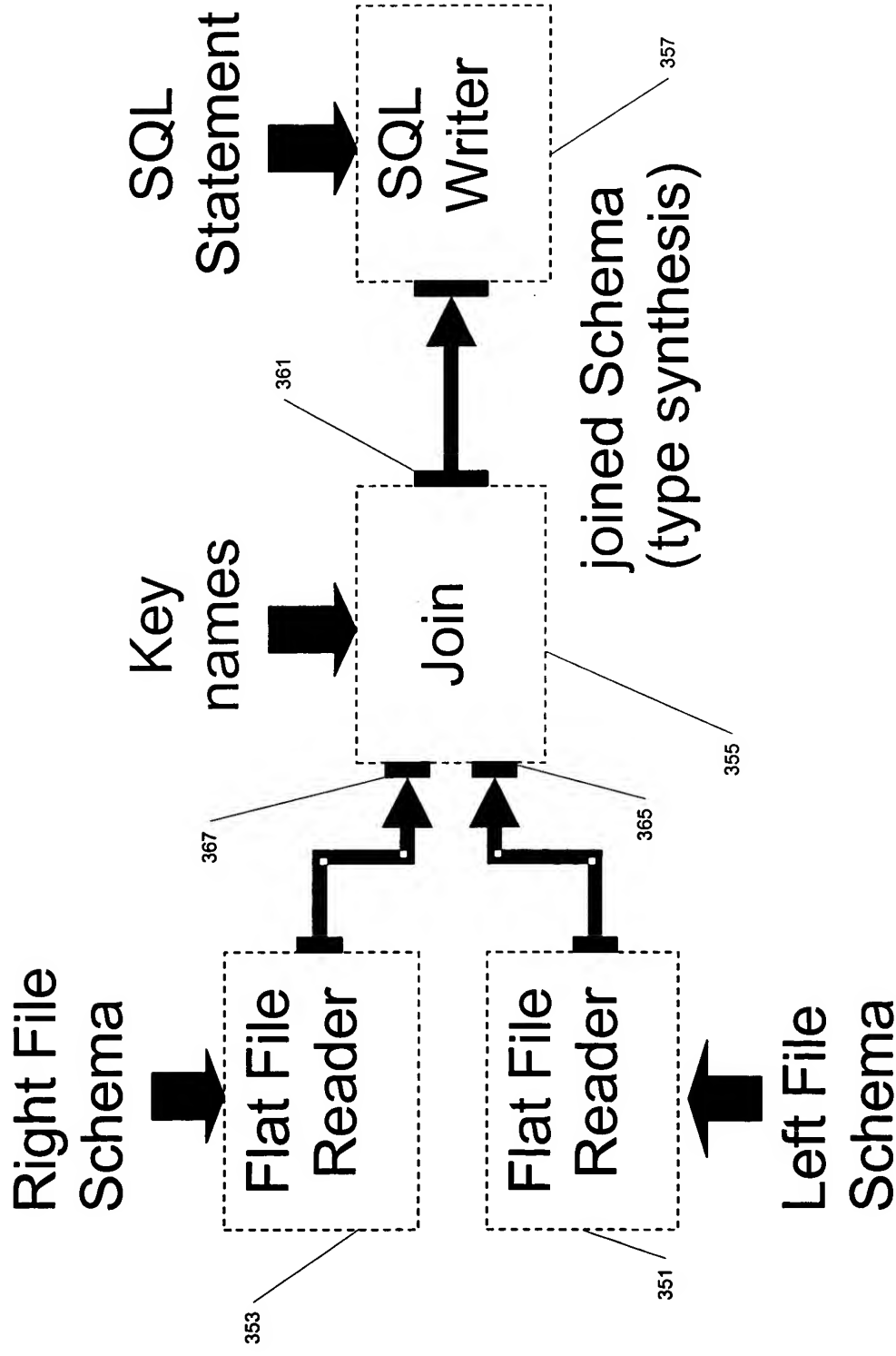
**Fig. 15**



**Fig. 16**



**Fig. 17**



Join Example

Fig. 18

Key names

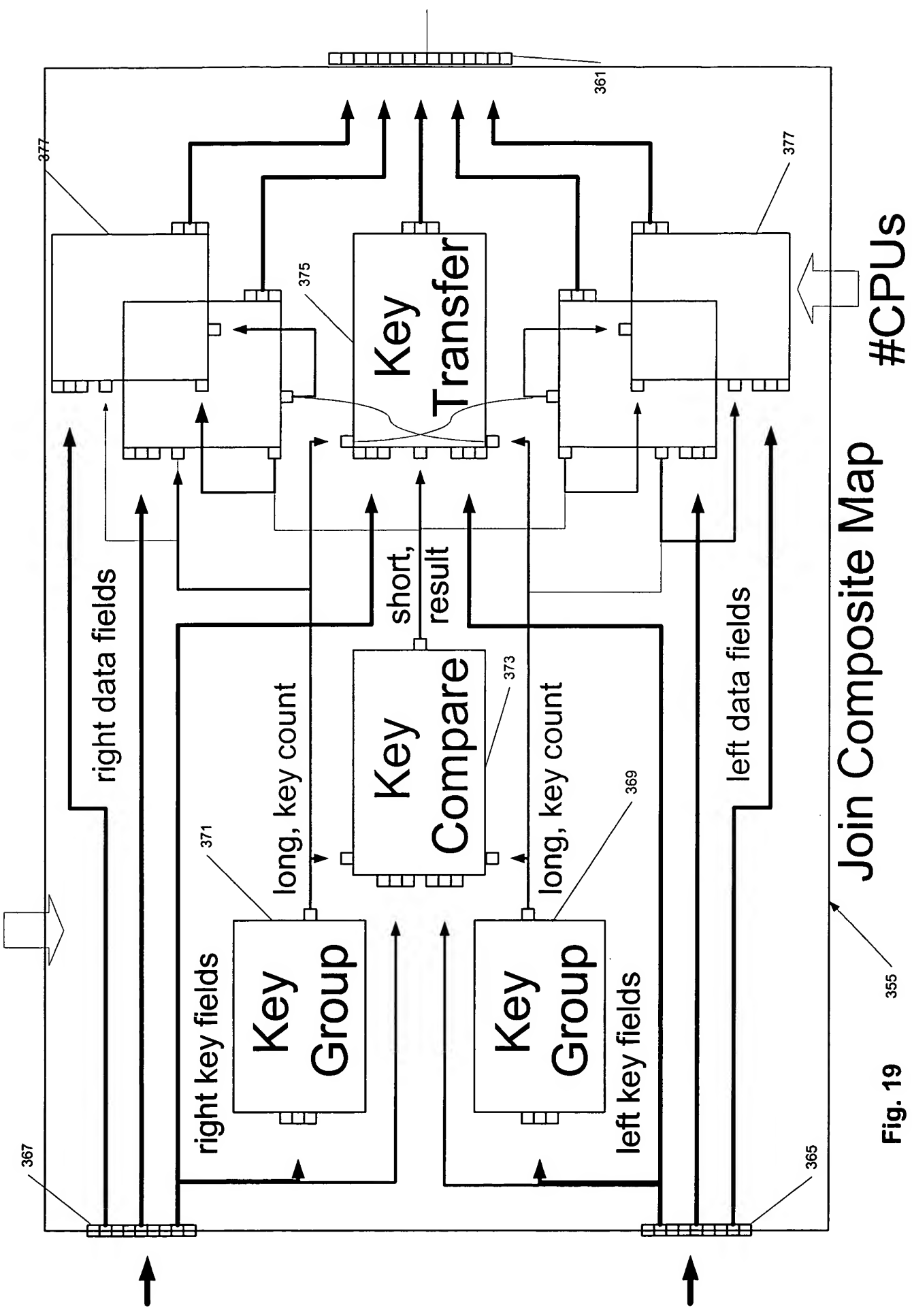
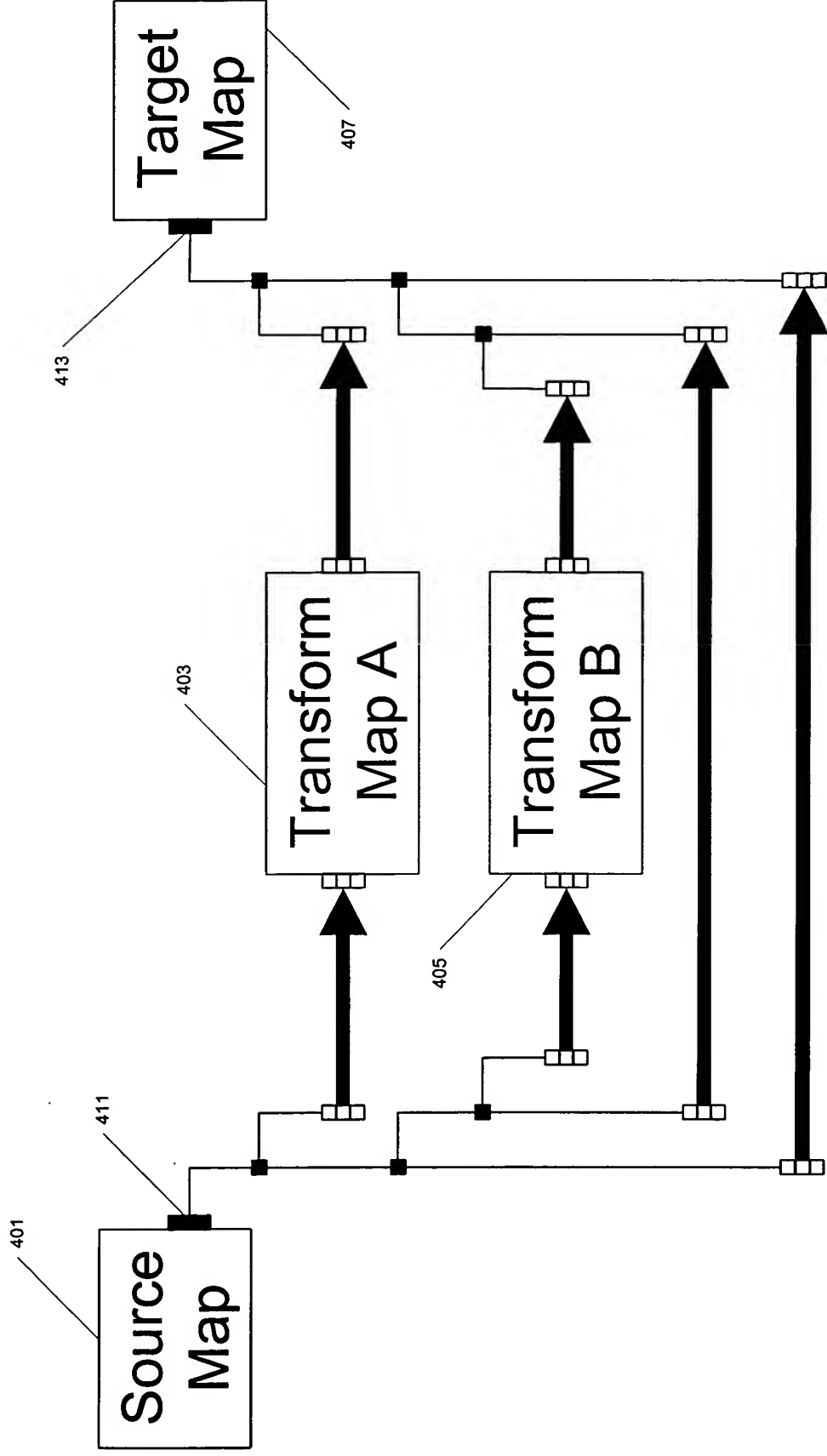
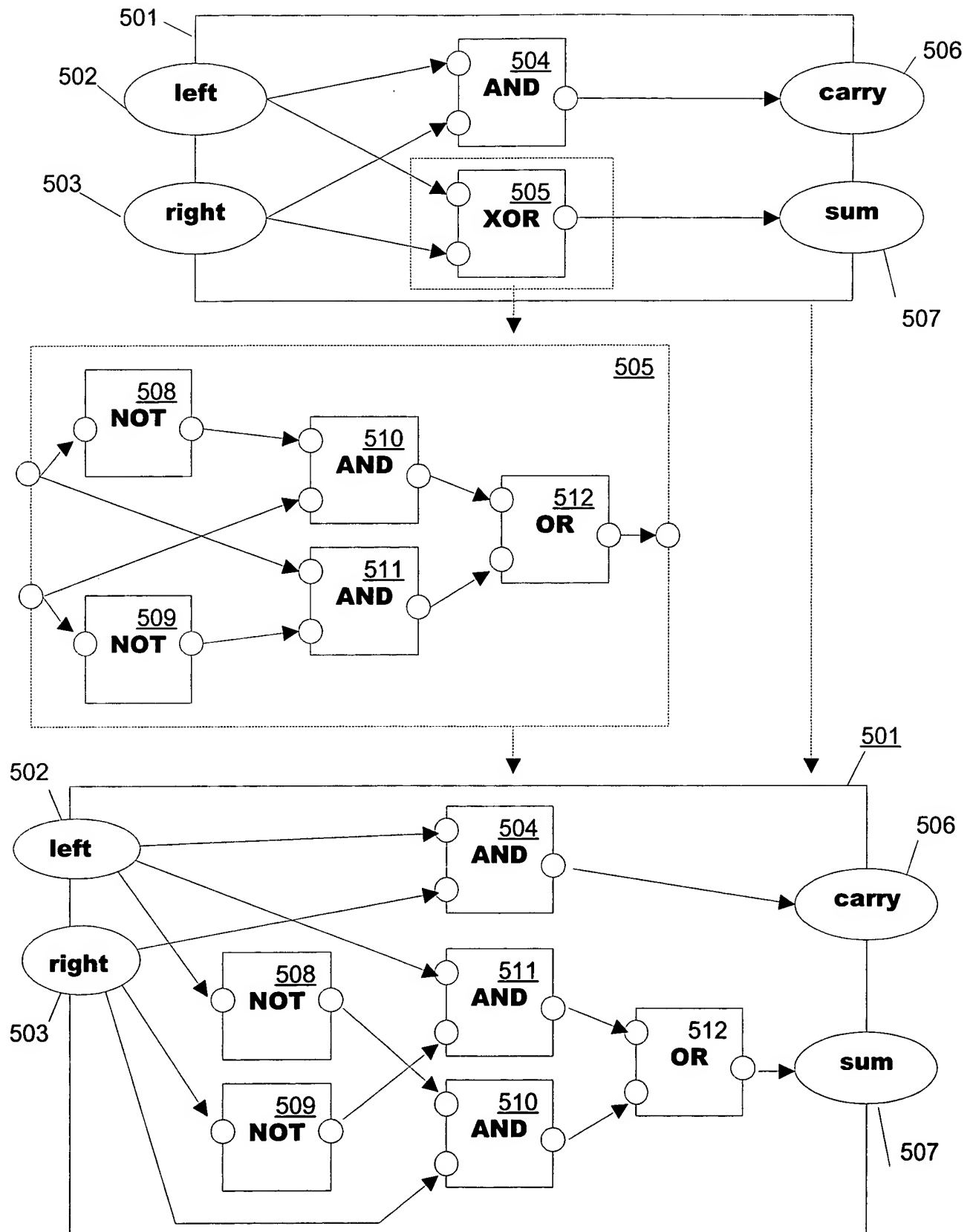


Fig. 19



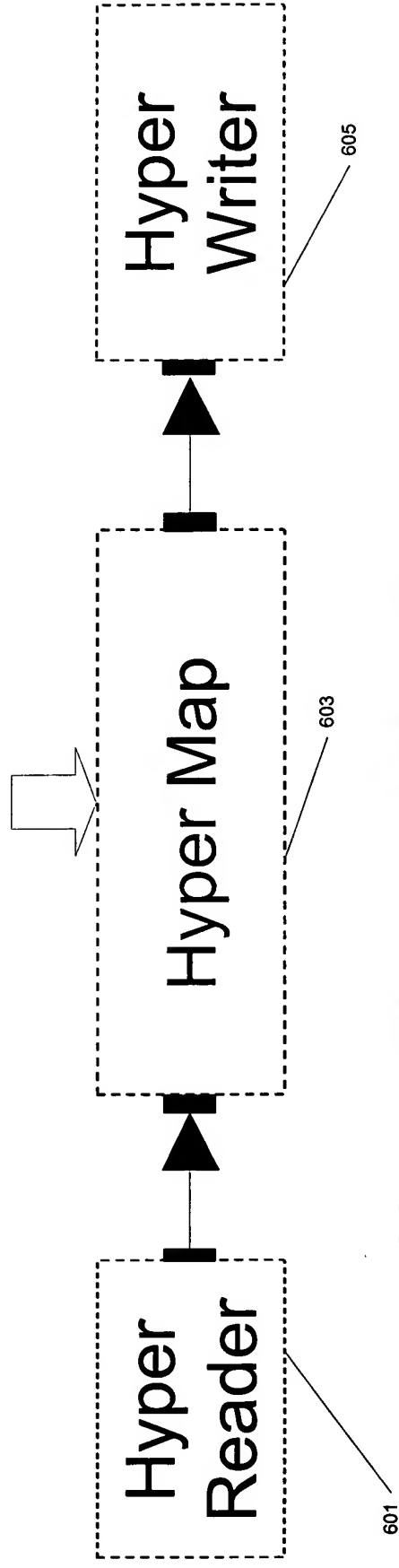
# Hierarchical Composite Ports

Fig. 20



**Fig. 21**

Transformation map  
+ properties



Hyper Map is a Map Template

Fig. 22



Transformation

map  
+ properties

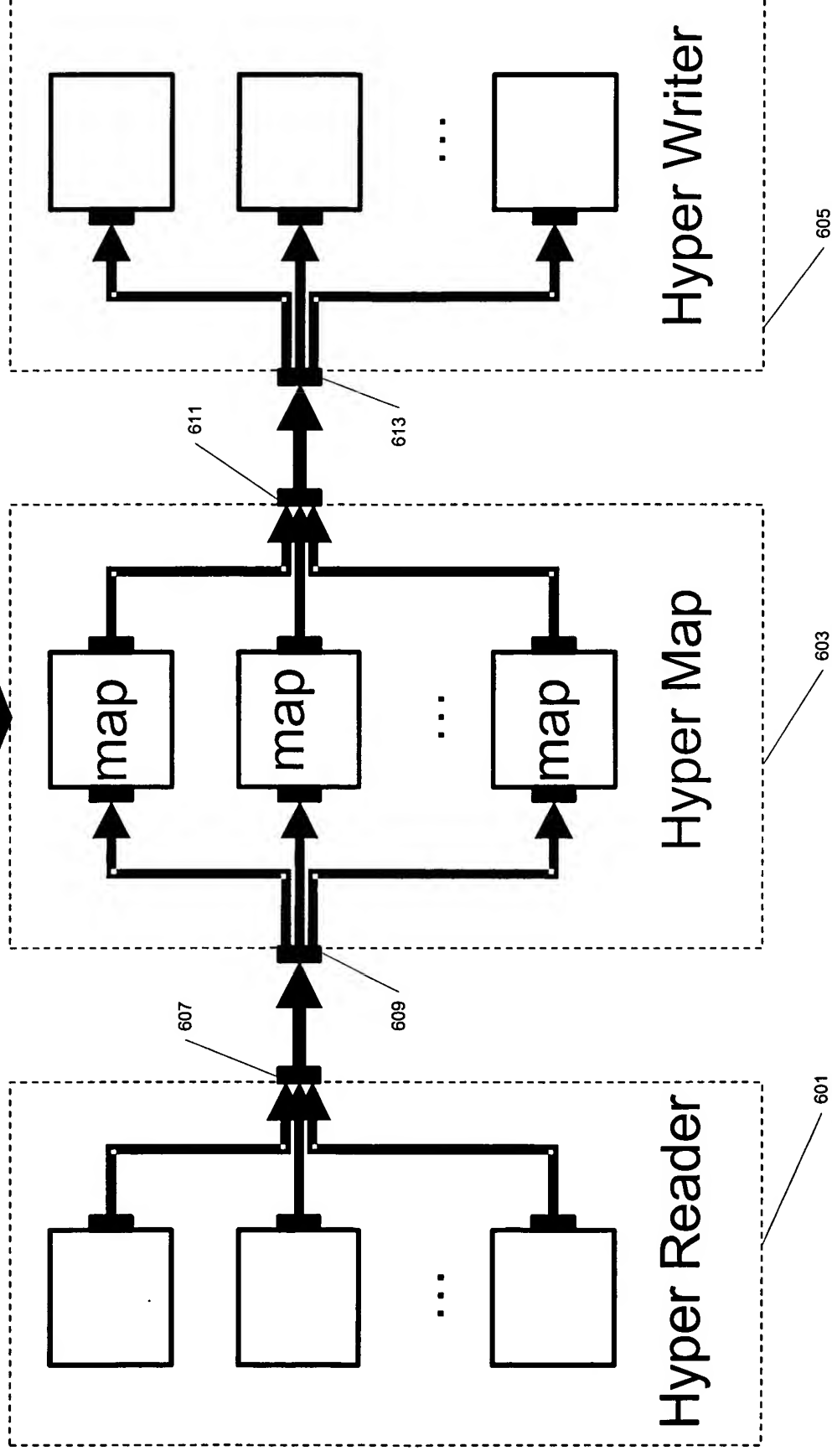


Fig. 23

Hyper Map Implements Partitioned Parallelism

Transformation map  
+ properties

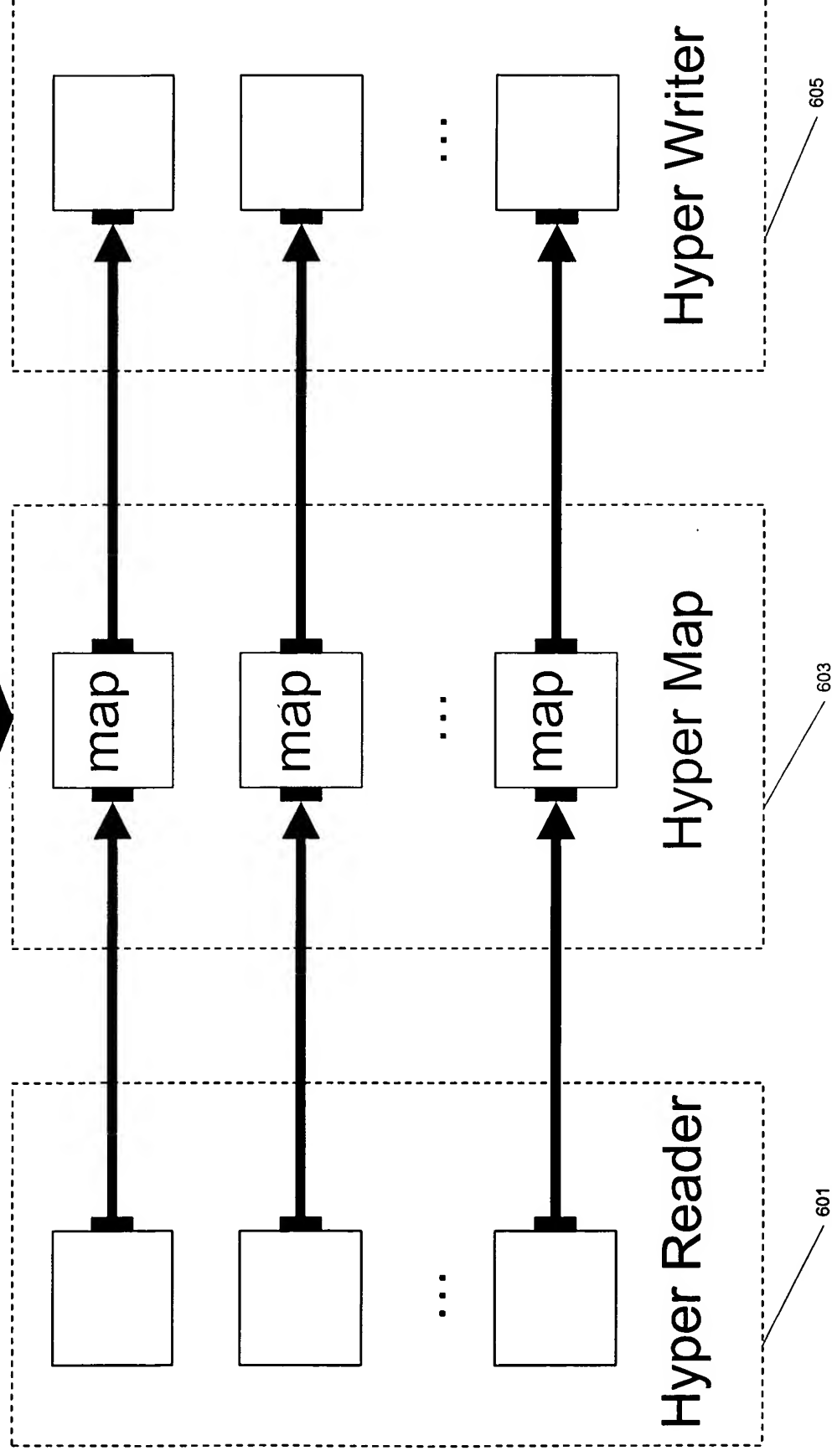


Fig. 24

Synthesis Trims Composite Map Links

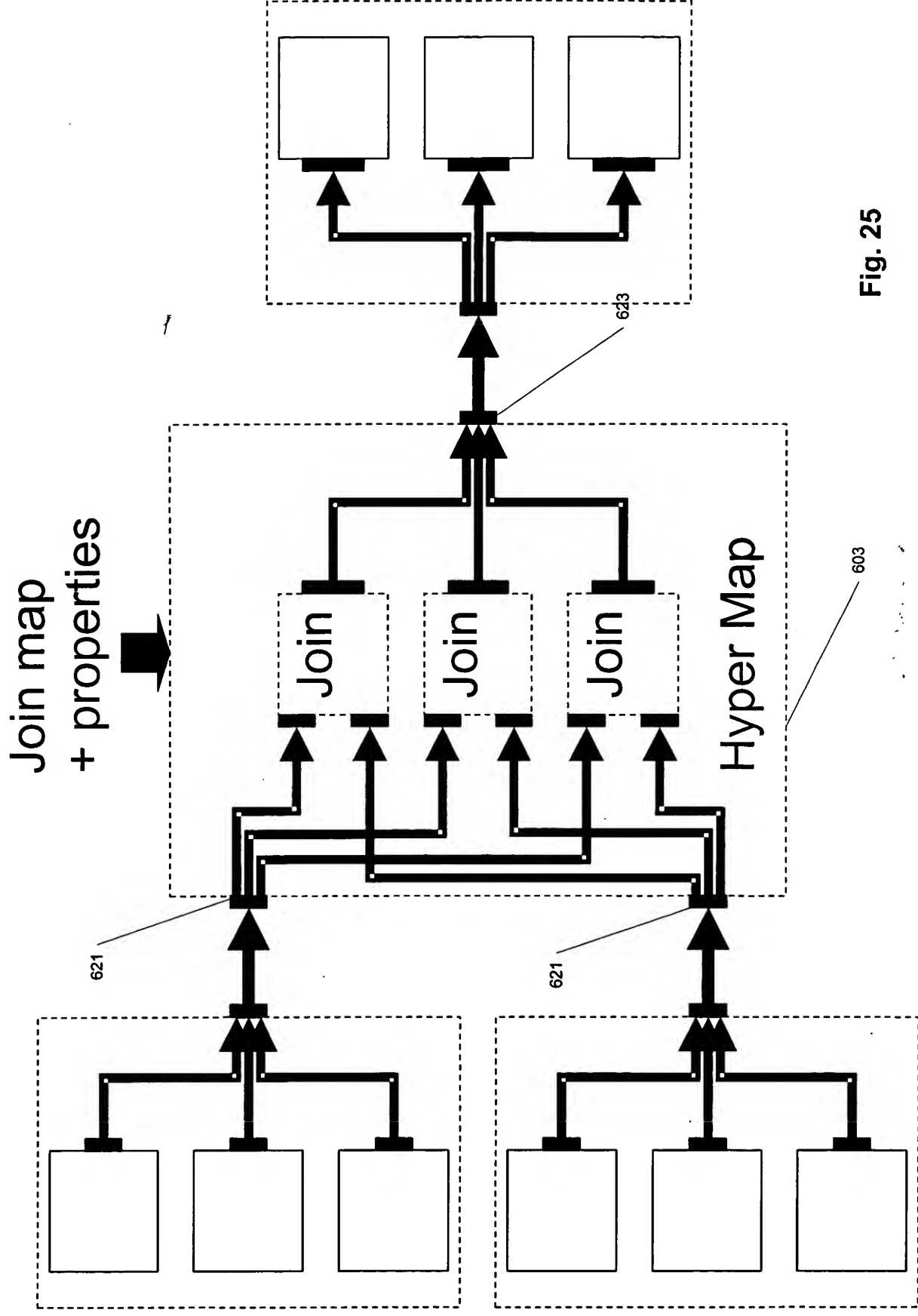


Fig. 25

Hyper Map Partitions another Map's Interface

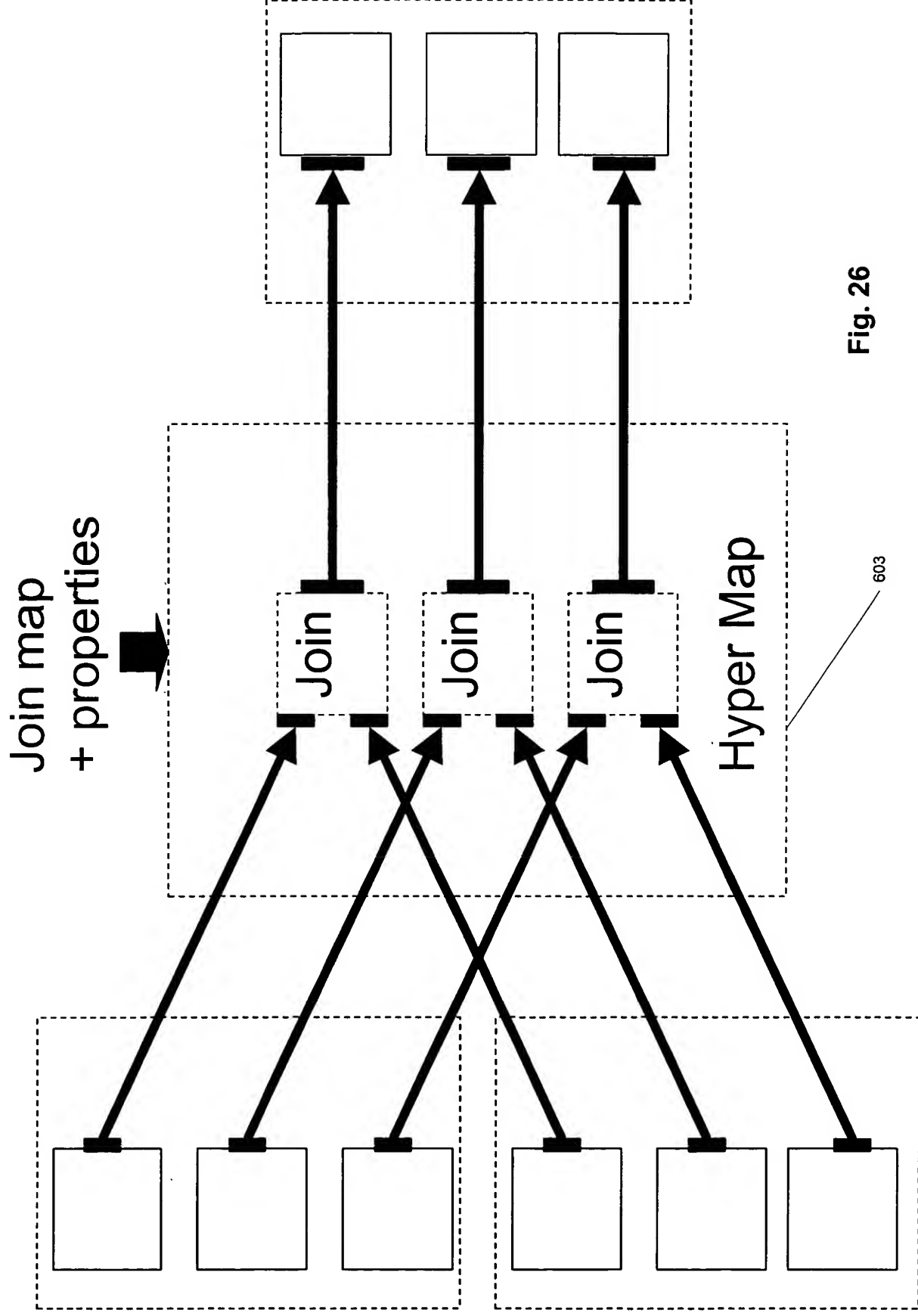


Fig. 26

Hyper Map Implements Partitioned Join

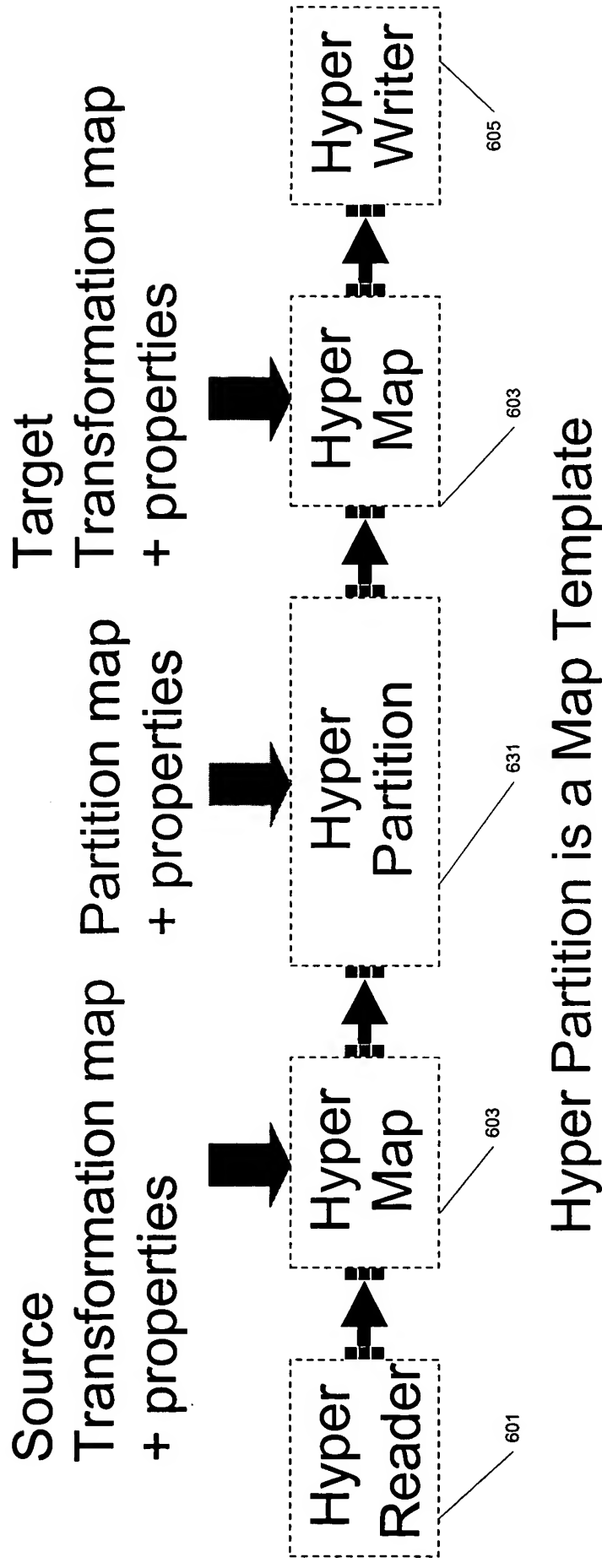
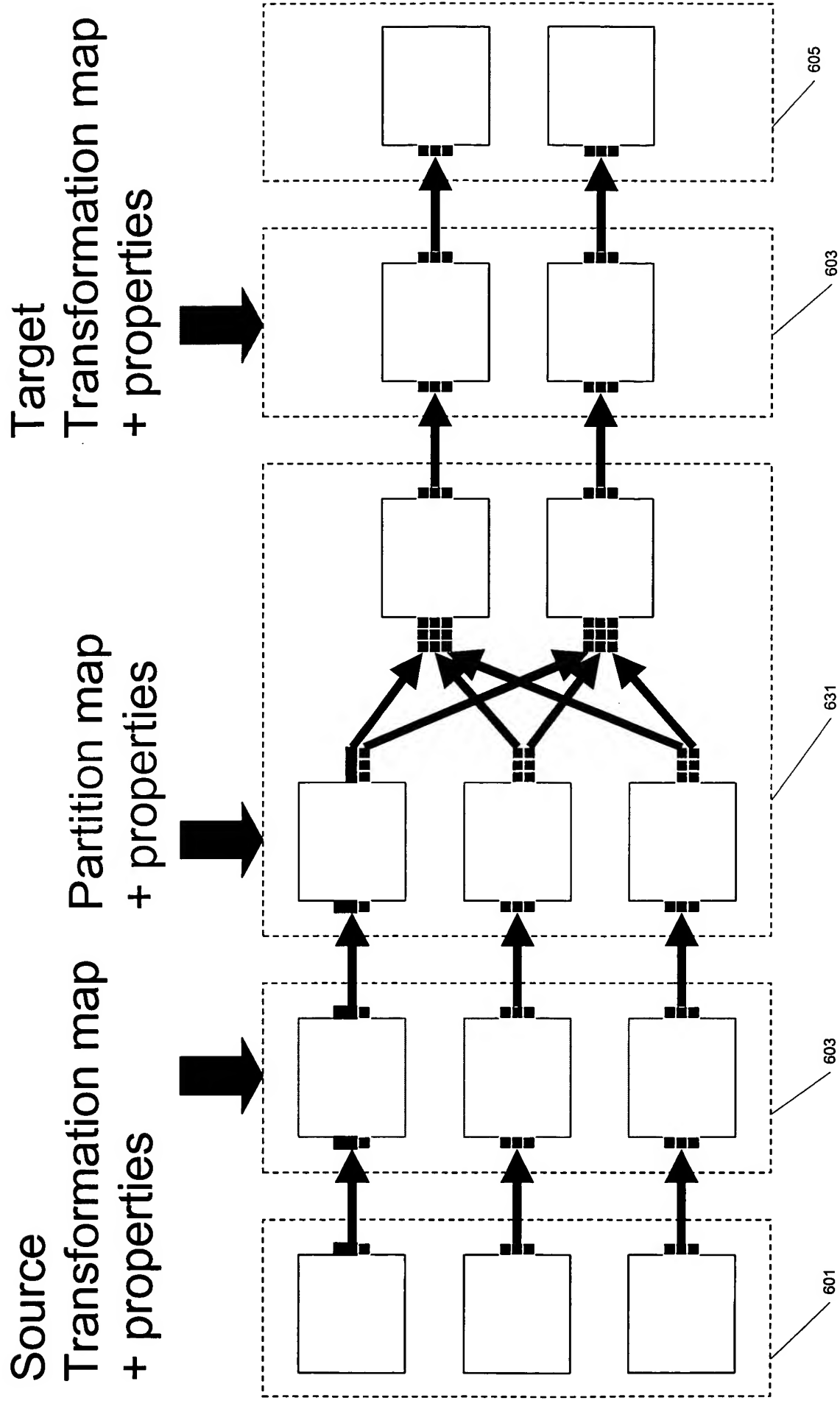


Fig. 27



Hyper Partition corrects Partition Schema Mismatch

Fig. 28

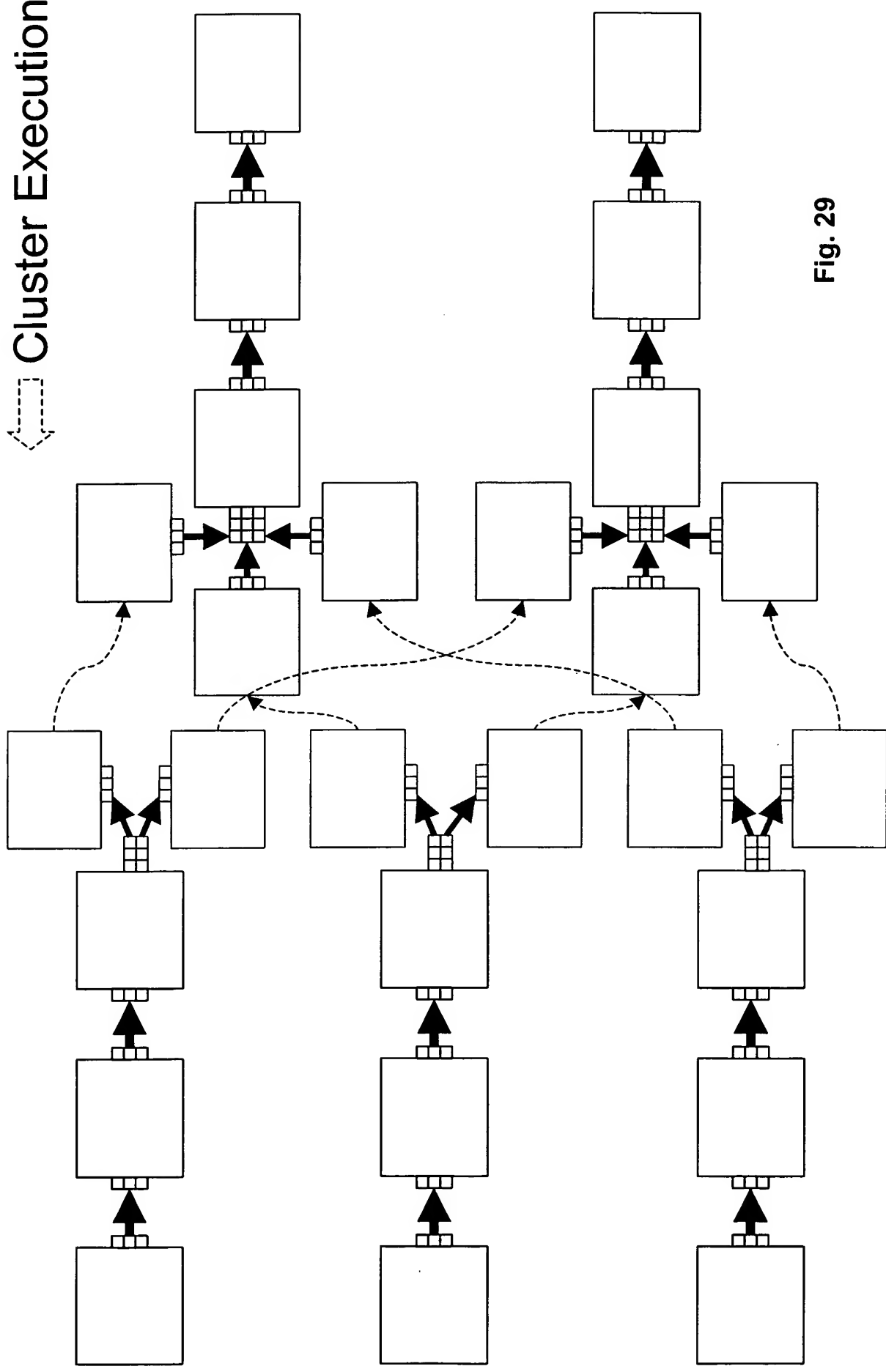


Fig. 29

Cluster Execution of Hyper Partition Pattern

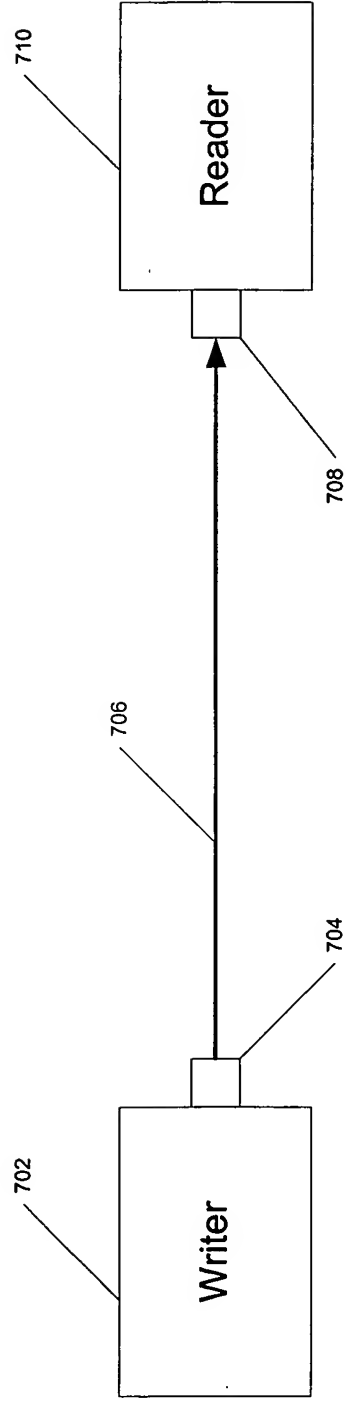


Fig. 30